## CORTEX M33 DE NXP FAMILIA LPC5500

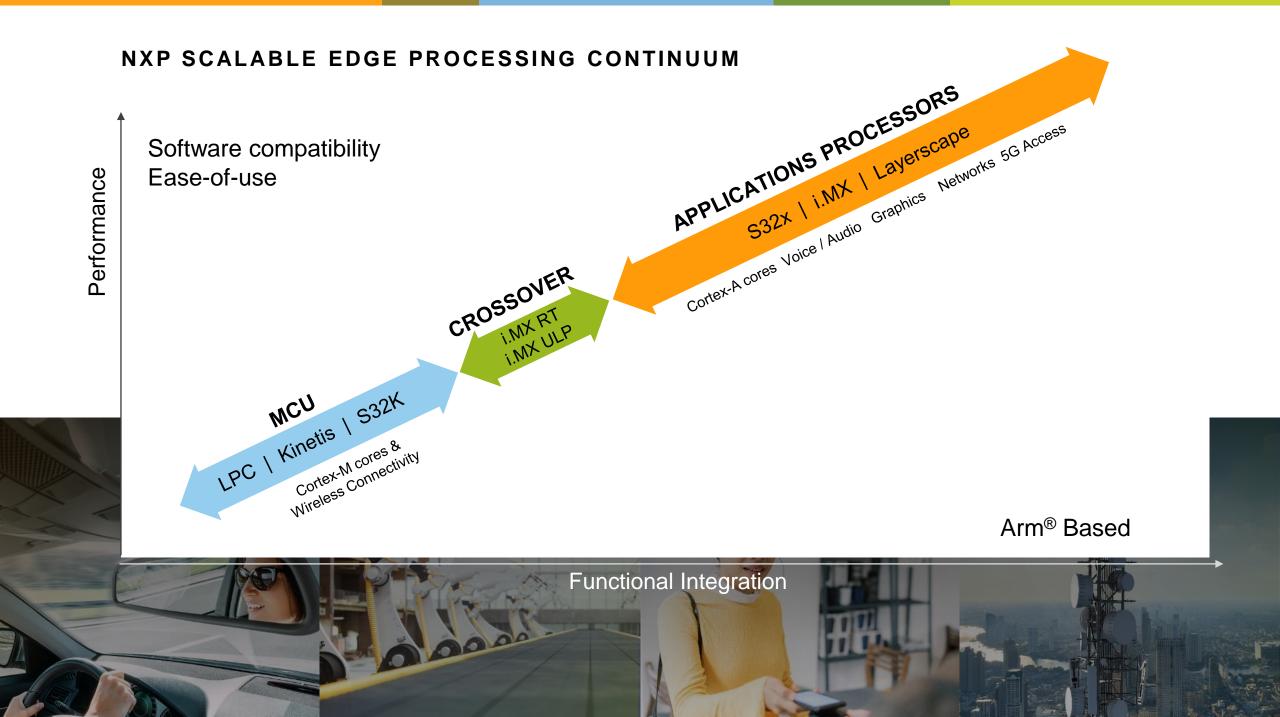




Electrocomponentes S.A. www.electrocomponentes.com







Cortex Maxin perform contro DS	num ance, I and	Trust	Zone	High performance
Cortex-M3	Cortex-M4	Cortex-M33	Cortex-M35P	
Performance efficiency	Mainstream control and DSP	Flexibility, control and DSP	Tamper resistance, flexibility, control and DSP	Performance efficiency
Cortex-M0	Cortex-M0+	Cortex-M23		
Lowest cost, low power	Highest energy efficiency	Smallest area, lowest power		Lowest power & area
Armv6-M	Armv7-M	Arn	nv8-M	

#### NXP LPC5500 MCU SERIES - INDUSTRY'S ONLY FULL ARMV8-M IMPLEMENTATION

#### **KEY FEATURES AND COMPARISONS**

 Nearly 20% performance improvement over Cortex-M4 based MCUs (over 60% vs Cortex-M0) with redesigned pipeline - up to two instructions per clock cycle

	Contex-M33
	TrustZone
	Stack limit checking
	Co-processor interface
	Enhanced debug
Cortex-M4	МТВ
ETM	ETM
NVIC (max 240 IRQs)	NVIC (max 480 IRQs)
MPU (PMSAv7)	MPU (PMSAv8)
AHB Lite	AHB5
FPU	FPU
SIMD/ DSP	SIMD/ DSP
WIC	WIC
Serial wire / JTAG	Serial wire / JTAG
ARMv7-M	ARMv8-M mainline
	New or updated

Cortex-M33

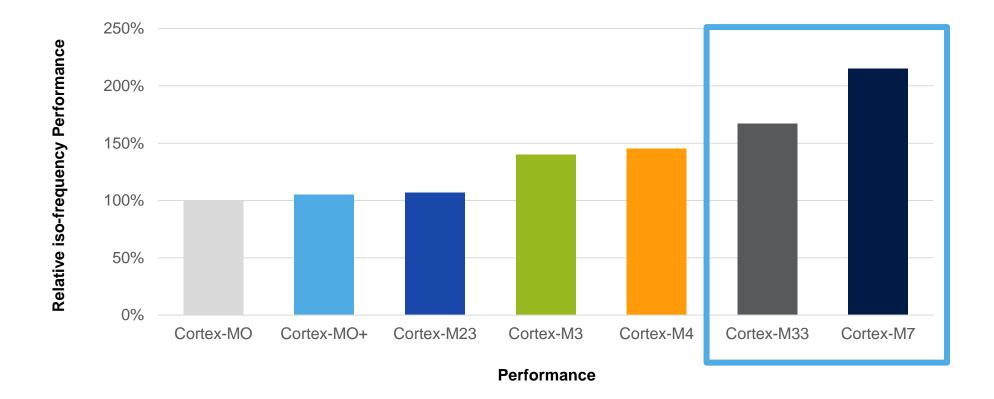
	CORTEX-M0+	CORTEX-M23	CORTEX-M3	CORTEX-M4	CORTEX-M33
DMIPS/MHz	0.95	0.98	1.25	1.25	1.50
CoreMark <sup>®</sup> /MHz	2.46	2.50	3.32	3.40	4.02

Prelim. Data from Arm for Cortex-M33 implementation at 40LP (9-track, typical 1.1v, 25°C)

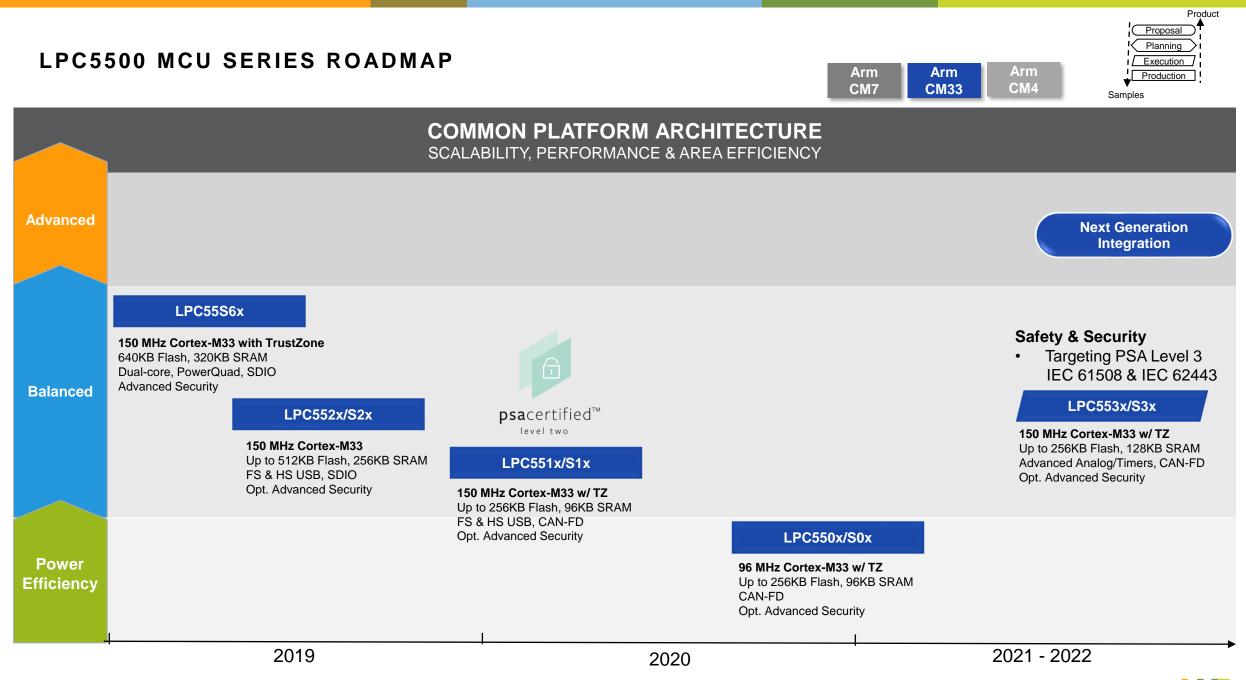
- Optimal balance between performance, power and security. With TrustZone, same energy efficiency as Cortex-M4. Binary compatible with Cortex-4 when TrustZone disabled
- Tightly coupled accelerators with coprocessor interface & extensions (Arm's single precision FPU along with NXP accelerators)
- TrustZone for system-wide, secure resource isolation enabling trusted runtime execution and physical protection in embedded MCU applications

#### **CORTEX-M7 – HIGHEST PERFORMANCE CORTEX-M CORE**





http://www.arm.com/-/media/arm-com/products/processors/Cortex-M-series-performance-graph.jpg?la=en



#### NXP LPC5500 MCU SERIES COMMON PLATFORM ARCHITECTURE FOR COMPLETE SCALABILITY

#### **Common features across families**

- FS/HS USB with PHY, 50MHz SPI, up to 8 Serial Interfaces (FlexComm)
- 5x 32b Timers, SCTimer, and FlexPWM (on LPC553x)
- Up to 2Msps 16-bit SAR ADC, Comparator, Temperature Sensor and RTC
- 1.8 to 3.6V, -40 to 105  $^\circ\text{C}$

LPC5500 Family	Samples [Launch]	Memory	Max Freq	Dual Core	Security	DSP Accel	USB*	SDIO	CAN- FD*	FlexSPI	I3C	DMIC	Analog**	Serial Interface
Adv. Analog LPC553x/S3x (S3x version available in Q1-23)	Now [Apr 22]	Up to 256KB Flash, 128KB SRAM	150 MHz w 8KB Cache Opt TZ	-	Opt.	Yes	FS	-	1x	1	1	2 ch	4x ADC 3x Analog Comparator 3x DAC 3x OpAmp	8x FlexComm, HS SPI
Efficiency LPC55S6x	Q4-18 [Mar-19]	Up to 640KB Flash, 320KB SRAM	150 MHz TZ	Yes	Yes	Yes	FS & HS	Yes	-		-		2x 16b ADC 1Msps	8x FlexComm, HS SPI
Mainstream LPC552x/S2x	Q3-19 [Sep-19]	Up to 512KB Flash, 256KB SRAM	150 MHz Opt TZ	-	Opt.	-	FS & HS	Yes	-		-		2x 16b ADC 1Msps	8x FlexComm, HS SPI
Entry LPC551x/S1x	Q4-19 [Feb-20]	Up to 256KB Flash, 96KB SRAM	150 MHz Opt TZ	-	Opt.	-	HS	-	1x		-		2x 16b ADC 2Msps	8x FlexComm, HS SPI
Baseline LPC550x/S0x	Q3-20 [Nov-20]	Up to 256KB Flash, 96KB SRAM	96 MHz Opt TZ	-	Opt.	-	-	-	1x		-		2x 16b ADC 2Msps	8x FlexComm, HS SPI

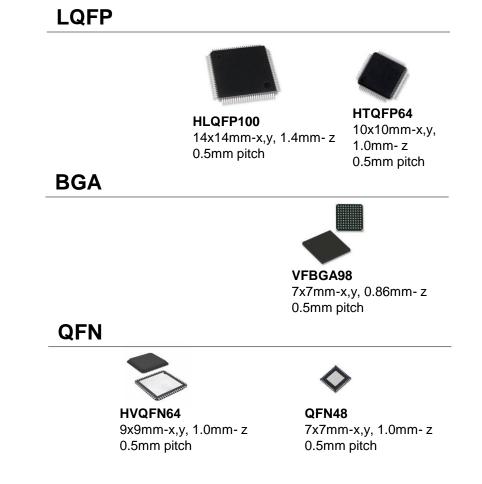
\*HS USB/CAN-FD not available on all part numbers within the family, check data sheet for specific configurations ; \*\*ADC specified for Single Ended configuration

#### NXP LPC5500 MCU SERIES - SCALABILITY

#### **Common features across families**

- FS/HS USB with PHY, 50MHz SPI, up to 8 Serial Interfaces (FlexComm)
- 5x 32b Timers, SCTimer, and FlexPWM (on LPC553x)
- Up to 2Msps 16-bit SAR ADC, Comparator, Temperature Sensor and RTC
- 1.8 to 3.6V, -40 to 105  $^\circ\text{C}$

LPC5500 Family	Memory	QFN 48	QFP 64	QFP 100	BGA 98	
Adv. Analog LPC553x/S3x	Up to 256KB Flash, 128KB SRAM	Х	х	Х		
Efficiency LPC55S6x	Up to 640KB Flash, 320KB SRAM		х	x	х	
<b>Mainstream</b> LPC552x/S2x	Up to 512KB Flash, 256KB SRAM		х	X patibility	х	
<b>Entry</b> LPC551x/S1x	256KB Flash, 96KB SRAM		х	<sup>o</sup> in Com	х	
<b>Entry</b> LPC550x/S0x	256KB Flash, 96KB SRAM	х	х			



Core P	latform	Tim	ers
Arm Cor Up to 15		5 x 32b Timers	SCTimer/PWM
· · · · · · · · · · · · · · · · · · ·	PU, FPU, SIMD	Multi-Rate Timer	Windowed WDT
Arm Cor Up to 1		RTC	Micro Timer
DSP	Crypto Engine	Interf	aces
Accelerator		8 x Flex Supports UART	
System Power		HS LSPI	SDIO
Single V <sub>dd</sub> power s reduced power conv	upply, POR, BOD, modes – DCDC	HS USB + PHY	FS USB + PHY
Clock Gene OSCs, System PL	eration Unit		
Secure DMA0 Up to 22ch	Secure DMA1 Up to 10ch	See	
Men	nory	Secu	-
FLA		AES-256	SHA-2
Up to 6		SRAM PUF	PRINCE
RA Up to 3	320KB	Secure Debug Auth.	RNG
RC Boot		PFR	UID
Programmal	ole Features	Ana	log
Programmab 6 input,		ADC 16b 1MSPS	ACMP
			Temp Sensor

#### **Core Platform** Up to 150MHz Cortex-M33 er • Up to 150MHz Cortex-M33 Coprocessors Multilayer Bus Matrix Memory РНҮ • Up to 320KB RAM

• 128KB ROM

#### Timers

• 5 x 32b Timers

- DSP Accelerator - Crypto Engine

• Up to 640KB FLASH

- SCTimer/PWM
- Muiti-Rate Timer
- Windowed Watchdog Timer

- TrustZone, MPU, FPU, SIMD

- RTC
- Micro Timer

#### Interfaces

- USB High-speed (H/D) w/ on-chip HS PHY
- USB Full-speed (H/D), Crystal-less
- SDIO, Support 2 cards
- 1 x High-Speed SPI up to 50MHz
- 8 x Flexcomms support up to 8x SPI, 8x I2C, 8x UART, 4x I<sup>2</sup>S channels (total 8 instances)

#### **Advanced Security**

- Protected Flash Region (PFR)
- AES-256 HW Encryption/Decryption Engine
- SHA-2

LPC55S6X PRODUCT BLOCK DIAGRAM

- SRAM PUF for Key Generation support
- PRINCE Real-time Encrypt/Decrypt for flash data
- Secure debug authentication
- RNG

#### Analog

- 1 16b ADC, up to 16ch, 1MSPS
- Analog Comparator
- Temperature Sensor

#### Packages

- HLQFP100
- VFBGA98
- HTQFP64

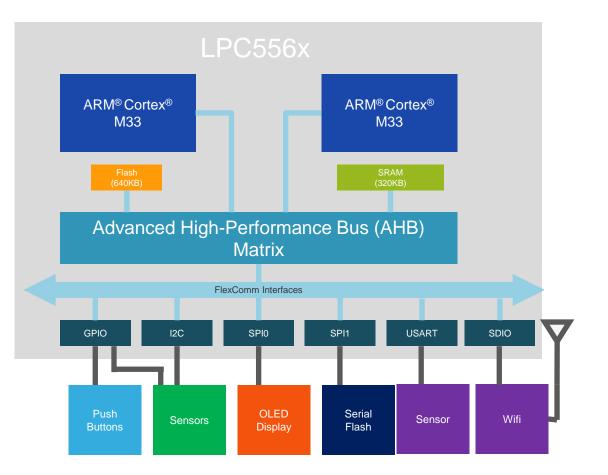
#### Other

- Programmable Logic Unit
- Buck DC-DC
- Operating voltage: 1.8 to 3.6V
- Temperature range: -40 to 105 °C
  - High Efficiency
  - Dual Core + Accelerators

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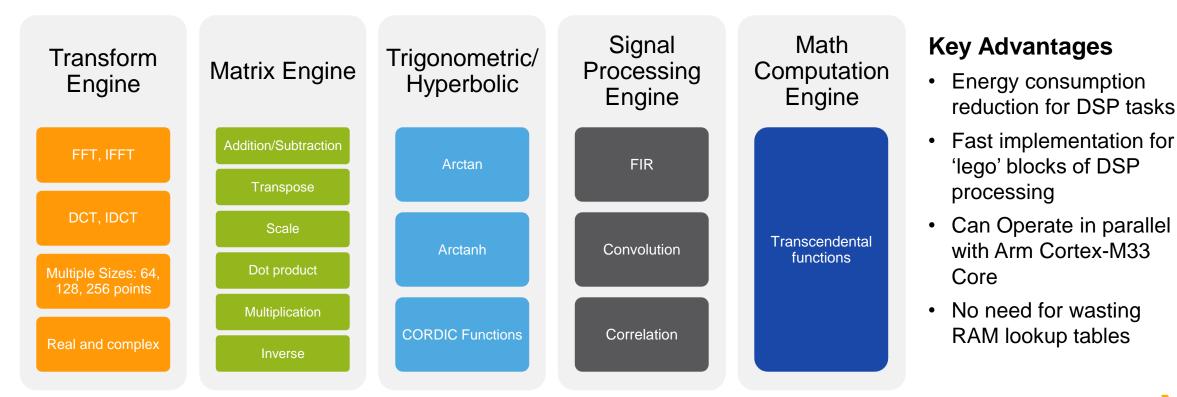
Advanced Security

- Dual Core
  - CPU0
    - Cortex-M33 with NVIC, FPU, MPU, DSP, ETM, SAU, TrustZone Security extension
    - Configured as primary CPU: Boots on Reset de-assertion, cannot be disabled
  - CPU1
    - Cortex-M33 with NVIC
    - Stays in reset until enabled by CPU0
  - Application partitioning
    - CPU1 can be leveraged for running system level tasks and the CPU0 can wake up to process data intensive tasks leveraging the co-processors
  - Ease of software development
    - Software development teams can develop code for each core independently allowing for a faster time to market



#### NXP'S POWERQUAD HARDWARE ACCELERATOR

- HW accelerator for frequently used math and signal processing computations
- ARM CMSIS-DSP API provides standardization for DSP code running on Cortex-M cores. Coprocessors can leverage this API
- <u>15x</u> more efficient than Cortex-M33 running CMSIS-DSP lib for FFT/IFFT (~50x faster than generic FFT C-code running on Cortex-M33)



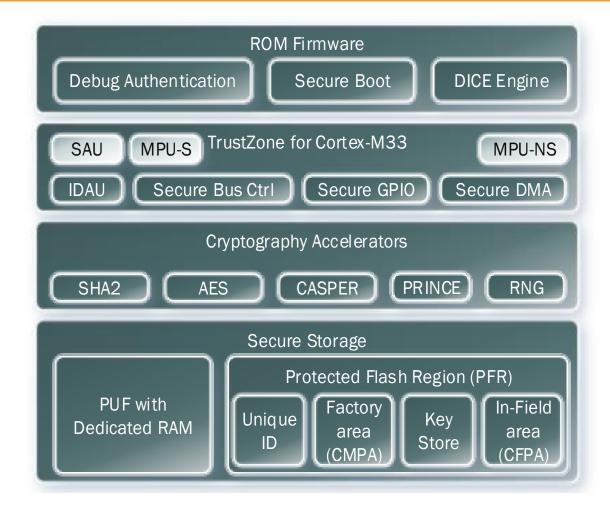


# CRYPTO-ENGINE IS PART OF THE SECURITY SUB-SYSTEM

	ROM Firmware
Debug Authenticatio	n Secure Boot DICE Engine
SAU MPU-S <sup>Tr</sup> IDAU Secure B	ustZone for Cortex-M33 MPU-NS us Ctrl Secure GPIO Secure DMA
Cr SHA2 AES	yptography Accelerators
	Secure Storage
PUF with Dedicated RAM	Protected Flash Region (PFR) Unique ID ID ID ID ID ID ID IN-Field Area (CFPA)

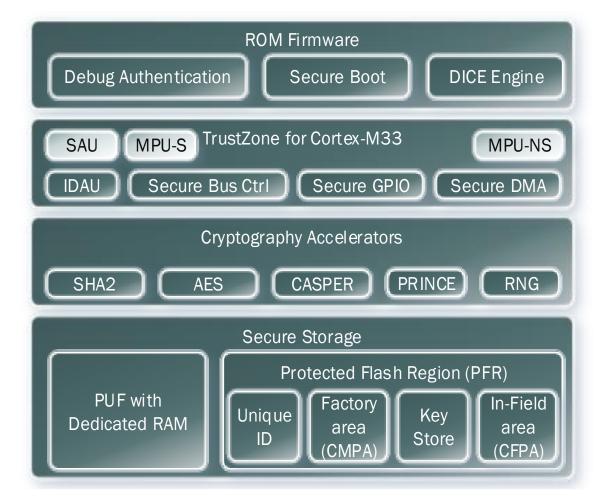
# NXP LPC5500 MCU SERIES LPC5586X SECURITY SUB-SYSTEM

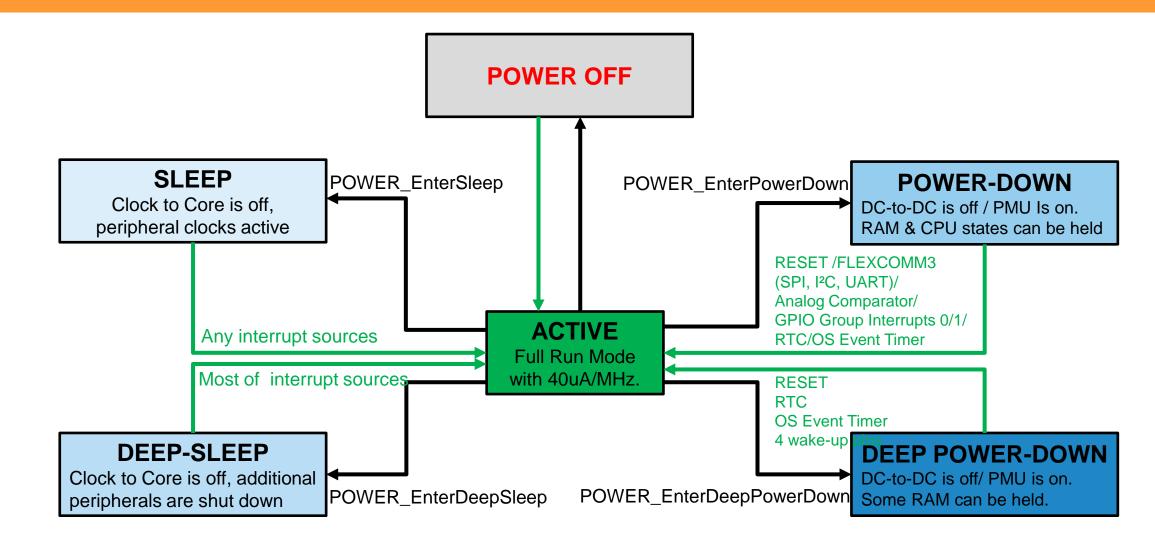
- ROM-based secure boot, debug authentication
- ARMv8M TrustZone-M with secure/non-secure MPU and Secure Attribution Unit (SAU)
- Implementation Defined Attribution Unit (IDAU), secure bus controller, secure DMA, and secure GPIO
- Secure storage:
- SRAM PUF (Physically Unclonable Function) for key generation and identity
- Protected Flash Region (PFR)



# NXP LPC5500 MCU SERIES LPC5586X SECURITY SUB-SYSTEM – CONT'

- AES-256 hardware symmetric encryption/decryption
   engine
- SHA-2 hash engine, supports SHA1 and SHA2
- PRINCE module On-The-Fly Encrypt/Decrypt for internal flash
- True Random Number Generator (TRNG)
- CASPER Crypto-Engine
- CASPER is a programmable compute engine it was designed to cope with the implementation challenges of asymmetric cryptography. CASPER provides acceleration for RSA, Diffie Helman and Elliptic Curve Cryptography and ECDSA signature generation







# PROGRAMMABLE FEATURES

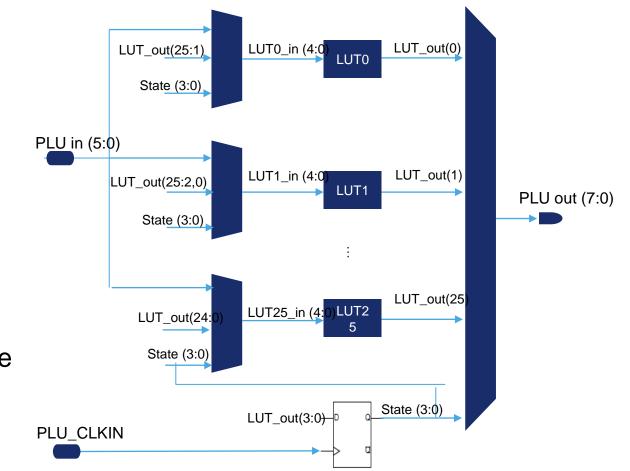
**Programmable Features** 

Programmable Logic Unit 6 input, 8 output



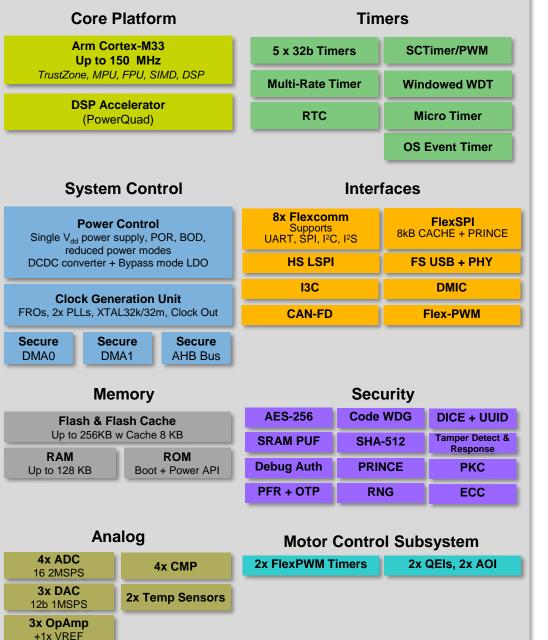
# NXP LPC5500 MCU SERIES

- Create combinational and sequential logic networks, simple state-machine
  - 26 Look-up Table (LUT)
    - 32-bit Truth Table
  - 6 inputs + 8 outputs to pad
  - Optional clock input
    - Required for sequential network
  - Supports interrupt and low power mode wakeup (deep-sleep only)



- Some potential functionality to implement in the PLU:
  - Integration of discrete logic device(s) to save cost and area
  - Event detection
  - Simple state machines
  - Stepper motor control
  - Generation of specialized waveforms / protocols in conjunction with other peripherals
- Benefits (vs function implementation on conventional MCU)
  - Low latency
  - Low power (can operate while MCU is in deep sleep)
  - Save MCU processing power for other tasks

#### LPC553X / LPC55S3X BLOCK DIAGRAM



#### **Core Platform**

- Up to 150MHz Cortex-M33
  - TrustZone, MPU, FPU, SIMD, DSP
- DSP Accelerator (PowerQUAD, w CP intf)
  - Secure Multilayer Bus Matrix

#### Memory

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٠

- Up to 256KB FLASH bank •
  - 8kB Low Power Cache
- Up to 128KB RAM
- 112KB with parity check
- 16KB ECC RAM
- ROM ٠

#### Timers

- 5 x 32b Timers ٠
- SCTimer/PWM
- Muiti-Rate Timer
- Windowed Watchdog Timer
- **RTC** with Calendar function
- Micro Timer
- OS Event Timer •

#### Analog

- 4x 16b ADC (Single ended) up to 23 ch
  - 2M sps 16bit
  - 3.3M sps 12bit
  - Up to 8 Differential/ 16 Single Ended channels
- **Temperature Sensor** ٠
- 3x Analog Comparator
- 3x 12b 1Msps DAC
- 3x OpAmp

#### Packages

- HVQFN48, HLQFP64, HLQFP100
  - VFBGA98 and CSP upon request

#### **Advanced Security**

- AES-256, SHA-2, RNG
- ECC-256 (ECDSA, ECDH) ٠
- PKC (Math accelerator) ٠
- SRAM PUF for Key Generation support ٠
- PRINCE real-time Encrypt/Decrypt for SPI flash ٠
- Debug authentication ٠
- Protected Flash Region (PFR)
- DICE and UID ٠
- Code Watchdog IP (CodeWDG) ٠
- Anti-tampering and Glitch Detector

#### Interfaces

- USB Full-speed (H/D), Crystal-less
- 1 x High-Speed SPI up to 50MHz (HS SPI)
- 8 x Flexcomms each supports SPI, I2C, UART, I<sup>2</sup>S
  - I2S Pin-sharing ٠
- External SPI -FlexSPI Interface support XIP ٠
  - Octal/Quad Flash
  - with 8kCache
  - PRINCE to encrypt & decrypt on the fly
- 1x CAN-FD
- 1x I3C
- 1x DMIC 2 ch .
- 2x FlexPWM with 4 sub-modules, providing 12 ٠ **PWM outputs**
- 2x Quadrature Encoder/Decoder (QEI) ٠

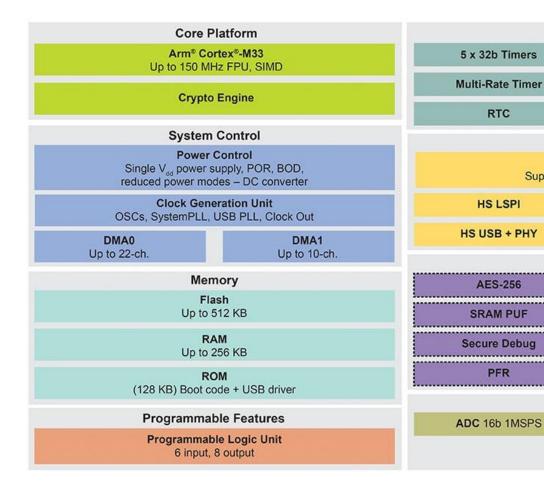
#### Other

- Buck DC-DC ٠
- Operating voltage: 1.8 to 3.6V ٠
- Two Main IO supplies (VDDIO 1: 1.8 V to 3.6 V, VDDIO\_2: 1.08 v to 3.6 V).
- Temperature range: -40 to 105 °C ٠





- ٠



#### **Advanced Security**

- Protected Flash Region (PFR)
- AES-256 HW Encryption/Decryption Engine
- SHA-2
- SRAM PUF for Key Generation support
- PRINCE Real-time Encrypt/Decrypt for flash data
- Secure debug authentication
- RNG

#### Analog

• 1 16b ADC, up to 16 ch, 1MSPS

Timers

Interfaces

8 x FlexComm

Supports UART, SPI, I2C, I2S

Security

Analog

SCTimer/PWM

Windowed WDT

Micro Timer

SDIO

FS USB + PHY

SHA-2

PRINCE

RNG

UID

ACMP

**Temp Sensor** 

- Analog Comparator
- Temperature Sensor

#### Packages

- HLQFP100
- VFBGA98
- HTLQFP64

#### Other

- Buck DC-DC
- Operating voltage: 1.8 to 3.6V
- Temperature range: -40 to 105 °C

### LPC552X/S2X PRODUCT OVERVIEW

#### **Core Platform**

- Up to 150MHz Cortex-M33
- Multilayer Bus Matrix

#### Memory

- Up to 512KB FLASH
- Up to 256KB RAM
- 128KB ROM

#### Timers

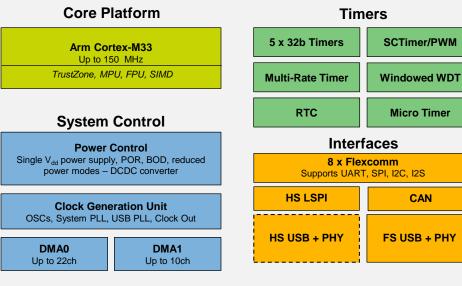
- 5 x 32b Timers
- SCTimer/PWM
- Muiti-Rate Timer
- Windowed Watchdog Timer
- RTC
- Micro Timer

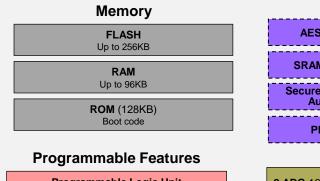
#### Interfaces

- USB High-speed (H/D) w/ on-chip HS PHY
- USB Full-speed (H/D), Crystal-less
- SDIO, Support 2 cards
- 1 x High-Speed SPI up to 50MHz
- 8 x Flexcomms support up to 8x SPI, 8x I2C, 8x UART, 4x I<sup>2</sup>S channels (total 8 instances)
  - High Efficiency Cortex-M33
  - Advanced Security
  - Rich Integration



#### LPC551X/S1X PRODUCT OVERVIEW





**Programmable Logic Unit** 6 input, 8 output

c	Micro Timer
Inter	faces
	<b>xcomm</b> T, SPI, I2C, I2S
SPI	CAN
+ PHY	FS USB + PHY
Sec	urity

#### **AES-256** SHA-2 SRAM PUF PRINCE Secure Debug RNG Auth. PFR UID Analog 2 ADC 16b 2MSPS ACMP

**Temp Sensor** 

#### Optional

#### **Core Platform**

- Up to 150MHz Cortex-M33
- Multilayer Bus Matrix

#### Memory

- Up to 256KB FLASH
- Up to 96KB RAM
- 128KB ROM

#### Timers

- 5 x 32b Timers
- SCTimer/PWM
- Muiti-Rate Timer
- Windowed Watchdog Timer
- RTC
- Micro Timer

#### Interfaces

- USB High-speed (H/D) w/ on-chip HS PHY USB Full-speed (H/D), Crystal-less
- 1 x High-Speed SPI up to 50MHz
- 8 x Flexcomms support up to 8x SPI, 8x I2C, 8x UART, 4x I<sup>2</sup>S channels (total 8 instances)
- CAN-FD

#### **Advanced Security**

- Protected Flash Region (PFR)
- AES-256 HW Encryption/Decryption Engine
- SHA-2
- SRAM PUF for Key Generation support
- PRINCE Real-time Encrypt/Decrypt for flash data
- Secure debug authentication
- RNG

#### Analog

- 1 16b ADC, up to 16 ch, 2MSPS
- Analog Comparator
- Temperature Sensor

#### Packages

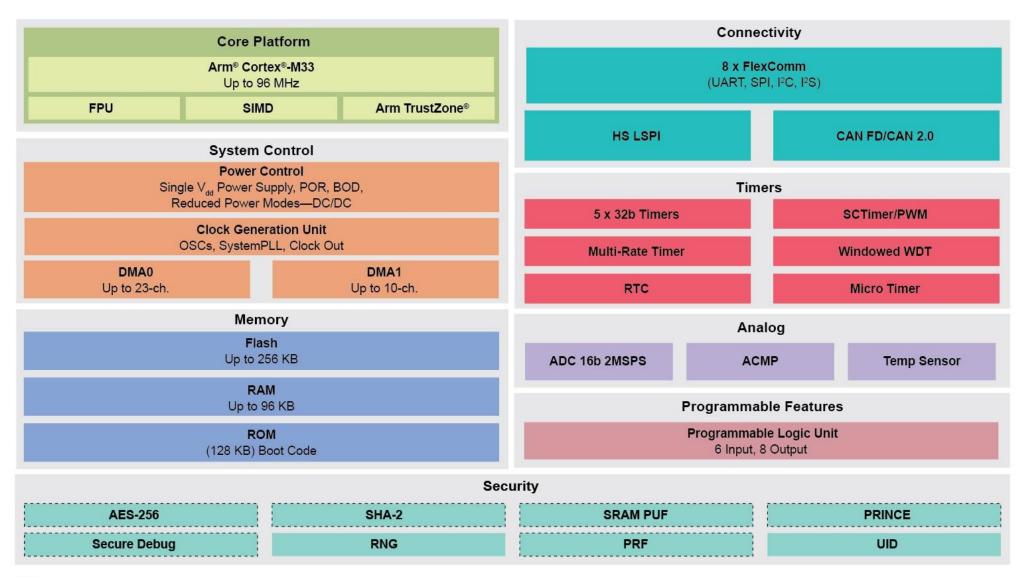
- LQFP100
- VFBGA98
- LQFP64

#### Other

- Buck DC-DC
- Operating voltage: 1.8 to 3.6V
- Temperature range: -40 to 105 °C
  - High Efficiency Cortex-M33

- Advanced Security
- CAN-FD and USB HS

#### LPC550X/S0X PRODUCT OVERVIEW



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#### LPC5500 MCU SERIES OVERVIEW

	LPC550x/S0x	LPC551x/S1x	LPC552x/S2x	LPC553x/S3x	LPC55S6x
Cortex-M33 Max Frequency	Up to 96MHz	Up to 150MHz	Up to 150MHz	Up to 150MHz & 8KB Cache	Up to 150MHz (w 2 <sup>nd</sup> M33)
Accelerators/ Co-proccessors	Crypto Accelerator	Crypto Accelerator	Crypto Accelerator	PowerQuad DSP, PKC	PowerQuad DSP, Crypto Accelerator
Flash	Up to 256 KB	Up to 256 KB	Up to 512KB	Up to 256KB	Up to 640KB
SRAM	Up to 96KB	Up to 96KB	Up to 256KB	Up to 112kB w Parity + 16kB ECC	Up to 320 KB
Security	TrustZone, HW SRAM PUF, Debug Authentication, real-time encryption/ decryption, TRNG, Secure boot, SHA-2, AES-256, PFR	TrustZone, HW SRAM PUF, Debug Authentication, real-time encryption/ decryption, TRNG, Secure boot, SHA-2, AES-256, PFR	HW SRAM PUF, Debug Authentication, real-time encryption/ decryption, TRNG, Secure boot, SHA-2, AES-256, PFR	CSS, TrustZone,HW SRAM PUF, Debug Authentication, real-time encryption/ decryption, TRNG, Secure boot, SHA-2, AES-256, PFR	TrustZone, HW SRAM PUF, Debug Authentication, real-time encryption/ decryption, TRNG, Secure boot, SHA-2, AES-256, PFR
CoreMarks	384	600	600	625	1150+ (Dual-core)
Serial Interfaces	Up to 8 FlexComm supporting USART, SPI, I2C and I2S. 1x HS LSPI	, Up to 8 FlexComm supporting USART, SPI, I2C and I2S. 1x HS LSPI	Up to 8 FlexComm supporting USART, SPI, I2C and I2S. 1x HS LSPI	Up to 8 FlexComm supporting USART, SPI, I2C and I2S. 1x HS LSPI	Up to 8 FlexComm supporting USART, SPI, I2C and I2S. 1x HS LSPI
USB	-	USB FS w/PHY, USB HS w/PHY	USB FS w/PHY, USB HS w/PHY	USB FS w/PHY	USB FS w/PHY, USB HS w/PHY
SDIO	-	-	SDIO/SD/MMC	-	SDIO/SD/MMC
FlexSPI				Support 2 SPI Flash or 1 Flash + 1 PSRAM	
CAN	CAN FD/ CAN 2.0	CAN FD/CAN 2.0	-	CAN FD/CAN 2.0	-
ADC	2x 16b 2 Msps	2x 16b 2 Msps	2x 16b 1 Msps	4x 16b 2 Msps (4x12b 3.13Msps)	2x 16b 1 Msps
GPIO	Up to 45	Up to 64	Up to 64	Up to 66	Up to 64
Active Power Consumption	32uA/MHz	32uA/MHz	32uA/MHz	57uA/MHz	32uA/MHz
Packages	HTQFP64, HVQFN48	HTQFP64, HLQFP100, VFBGA98	HTQFP64, HLQFP100, VFBGA98	HTQFP64, HLQFP100, QFN48	HTQFP64, HLQFP100, VFBGA98

#### LPC5500 MCU SERIES EVALUATION BOARDS FOR EASE OF DEVELOPMENT

- LPC55S69-EVK, LPC5536-EVK, LPC55S28-EVK, LPC55S16-EVK, LPC55S06-EVK
- Family fully featured part at up to 150 MHz
- High and full speed USB ports with micro A/B connector for host or device functionality.
- High- and full-speed USB ports\*
- Stereo audio codec\*
- NXP Accelerometer
- Arduino, Pmod & MikroE Click expansion options
- High speed on-board debug probe w/ UART/SPI/I2C bridging and option for J-Link firmware
- MicroSD card slot for families with SDIO\*\*
- On-board CAN-FD transceiver\*\*\*
- PCB layout, schematic and board files available

## Full set of drivers, middleware and examples available in MCUXpresso SDK

\*On LPC55S16-EVK, LPC55S28-EVK and LPC55S69-EVK

\*\* On LPC55S28-EVK and LPC55S69-EVK













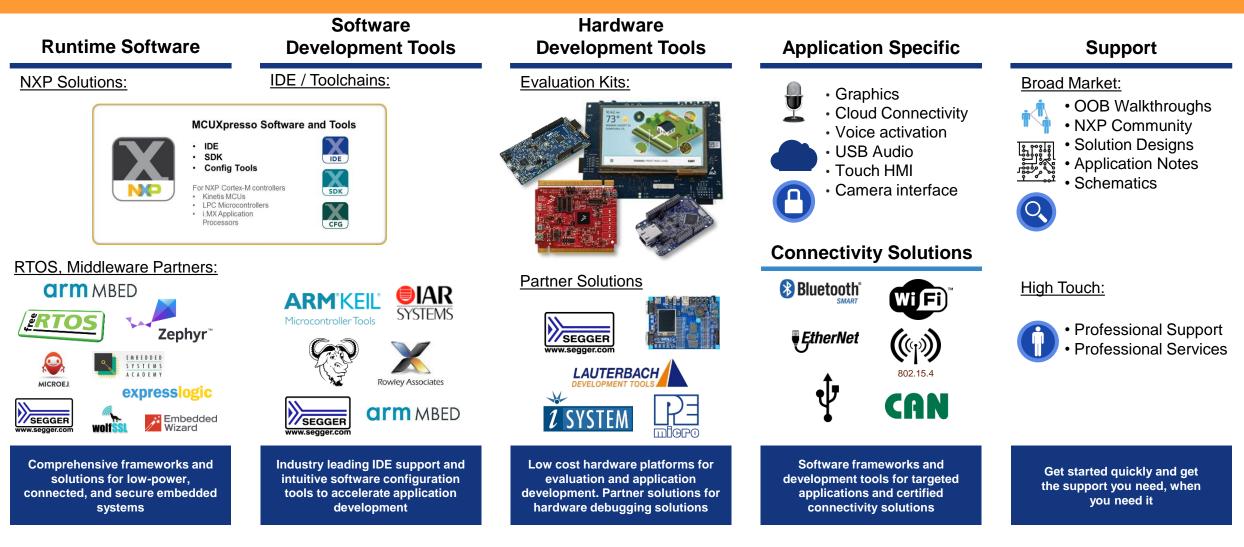


# PART III - ENABLEMENT





# NXP LPC5500 MCU SERIES NXP MCU SOFTWARE AND ENABLEMENT OVERVIEW



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## NXP LPC5500 MCU SERIES MCUXPRESSO SOFTWARE & TOOLS — PRODUCTS

#### Integrated Development Environment (IDE

- Offers edit, compile, debug, optimize, and many more tools with an intuitive and powerful interface
- Brings "best of" legacy IDEs (LPCXpresso and Kinetis® Design Studio) together, including GNU tool integration and library, multicore capable debugger, as well as trace functionality
- Debug connections that support all Freedom, Tower®, and LPCXpresso development boards plus industry leading commercial debug probes

#### Software Development Kit (SDK)

IDE

SDK

CFG

- The software framework and reference for application development with NXP's MCUs based on ARM® Cortex®-M cores
- Includes production-grade software with integrated RTOS, integrated stacks and middleware, reference software, and more
- Highest quality with MISRA compliance on all drivers; checked with Coverity® static analysis tools
- Available in custom downloads based on user selections of MCU, evaluation board, and optional software components

#### System Configuration Tools

- Integrated configuration and development tools for Kinetis, LPC and i.MX products
  - A suite of evaluation and configuration tools that helps guide users from first evaluation to production software development
- Includes SDK builder, pins, clocks and peripherals tools
- Available in online and desktop versions, and fully integrated into the MCUXpresso IDE

# NXP LPC5500 MCU SERIES **MCUEXPRESSO IDE**





Free Eclipse and GCC-based IDE for C/C++ development on Kinetis and LPC MCUs and i.MX RT crossover processors

	Integ	grated MCUXpress	o Confia Tools – P	ins, Clocks, Peri	oherals			
Quicks Pane	start	Support for SDK and LPCOpen for		Peripheral View	Power Measuremen			
Advan Build S		ARM® Cortex®-M Cores	Combined Development Perspective	Instruction Trace		O Trace/ rofiling		
New Project Wizard		Linker and Memory Configuration	1 cropective	Data Watching		TOS Kernel areness		
	ARM G	cc			ARM GDB			
newlib newl		Redlih		CMSIS-DAP	P&E	SEGGER		

### **Product Features**

- Feature-rich, unlimited code size, optimized for easeof-use, based on industry standard Eclipse framework for NXP's Kinetis and LPC MCUs and i.MX RT crossover processors
- Application development with Eclipse and GCCbased IDE for advanced editing, compiling and debugging
- Supports custom development boards, Freedom, Tower and LPCXpresso boards with debug probes from NXP, P&E and Segger
- Advanced Trace Features, including instruction trace, SWO trace and profiling
- **Free**: Full Featured, unlimited Code Size, no special activation needed, community based support

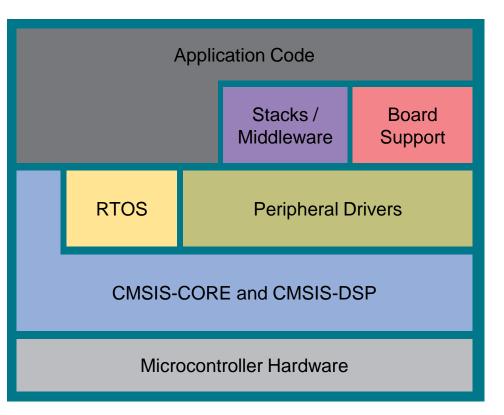
Learn more at: <u>www.nxp.com/mcuxpresso/ide</u>

## NXP LPC5500 MCU SERIES MCUEXPRESSO SDK





The software framework and reference for Kinetis & LPC MCU and i.MX RT application development



## **Product Features**

Architecture:

- **CMSIS-CORE** compatible
- Single driver for each peripheral
- Transactional APIs w/ optional DMA support for communication peripherals

#### Integrated RTOS:

- FreeRTOS v9
- **RTOS-native driver wrappers**

#### Integrated Stacks and Middleware:

- USB Host, Device and OTG
- IwIP, FatFS, LittleFS
- Crypto acceleration plus wolfSSL & mbedTLS
- SEGGER emWIN graphics library
- AWS IoT and Azure IoT
- SD and eMMC card support

#### Reference Software:

- Peripheral driver usage examples
- Application demos
- FreeRTOS usage demos

#### License:

BSD 3-clause for startup, drivers, USB stack

#### Toolchains:

- MCUXpresso IDE
- IAR®, ARM® Keil®, GCC w/ Cmake

#### Quality:

- Production-grade software
- MISRA 2004 compliance
- Checked with Coverity® static analysis tools





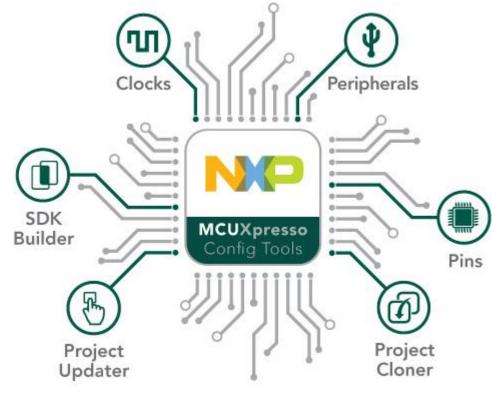




# NXP LPC5500 MCU SERIES MCUXPRESSO CONFIG TOOLS



Integrated configuration and development tools for LPC and Kinetis MCUs and i.MX RT crossover processors



**MCUXpresso Config Tools** is a suite of evaluation and configuration tools that helps guide users from first evaluation to production software development.



**SDK Builder** packages custom SDKs based on user selections of MCU, evaluation board, and optional software components.



**Pins, Clocks**, and **Peripherals** tools generate initialization C code for custom board support. Features validation of inputs and cross-tool conflict resolution.



**Project Updater** works directly with existing SDK-based IDE projects with generated Pins, Clocks, and Peripheral source files.



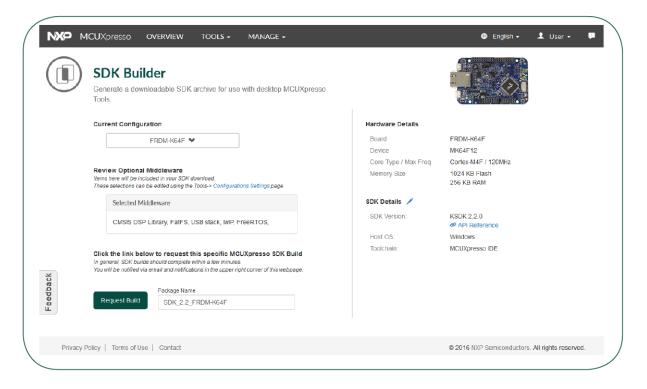
**Project Cloner** creates a standalone SDK project based on a example application available within SDK release.





#### SDK BUILDER

The MCUXpresso SDK Builder generates a downloadable SDK archive based on user selections of device, development board, toolchain, host OS, middleware and more. With a few simple configuration selections, the MCUXpresso SDK is ready for download and use with desktop MCUXpresso software and tools. These custom packages are inherently smaller in size and make the MCUXpresso SDK much more manageable than other "one size fits all" SDKs.





# NXP LPC5500 MCU SERIES **MCUXPRESSO CONFIG TOOLS – PINS TOOL**

#### **PINS TOOL**

The MCUXpresso Pins Tool is used for pin routing configuration, validation, and code generation. It provides pin settings for signal muxing, electrical properties, and run-time configurations. Selections can be easily captured using the graphical package view or searchable/ sortable spreadsheet view. The MCUXpresso Pins Tool generates easy to read ANSI-C initialization code suitable for C or C++ projects.

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32	ADC0_SE18/PTE	J2[18]/U8[6]/I2C	ACCEL_SDA	PTE25 U	ART4_RX		PTO8 -	CMT	DACO		DMA:	- VDD	080	*			
33	PTE26	J2[1]/D12[4]/LE	LED_GREEN	PTE26 U	ART4_CTS_6		ADC1_SE45/	ENET	BOM		Et Port	- F0.0	0_TX01 0_TX00			in binary form must is and the following	
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2 39	PTA5/USB_CLKL	U13[17]/RM00_R	RMD0_RXER	PTA5		FI	ADDI_SE7NPTC117	F IMZ BPIOB	FIME		GPICA	- FUU	D_AKDO	*			
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45	PTA15/SPID_SCK	U13[19]/RMID_T	RMB0_TXEN	PTA15 U	JARTO_RX		V0D140	PD B0	REM		RTC	PTA	a/			OVIDED BY THE COPY	
46	PTA16/SPID_SO	U13[20]/RMID_T	RM00_TXD0	PTA16 U	ARTO_CTS_b[]	=	PTC16/UART3_R0/	BDHC	SIM		SPID	PTA	ØUARTD U/UARTD			IED WARRANTIES, IN ANTABILITY AND FIT	
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<b>~</b> 54	ADC0_SE9/ADC	U13[11]/RM00	RMID_MDC	PTB1		FI	PTD4/LLWU_P14/	VREF				- BD	AL32				
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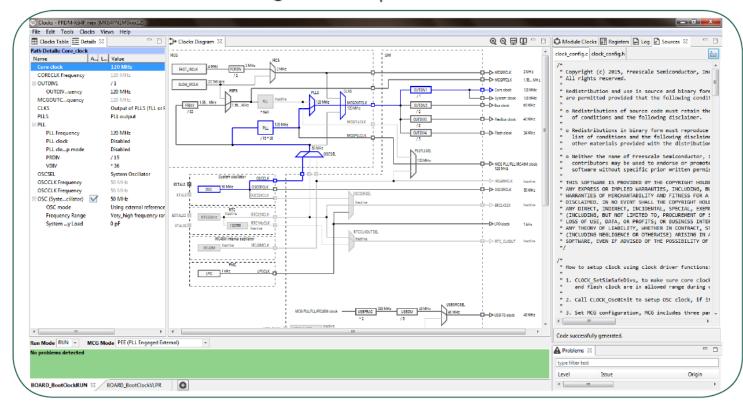


# NXP LPC5500 MCU SERIES **MCUXPRESSO CONFIG TOOLS – CLOCKS TOOL**

#### **CLOCKS TOOL**

The MCUXpresso Clocks Tool allows the user to easily configure the initialization of the system clocks (core, system, bus, peripheral clocks) and to generate C code with MCUXpresso SDK clock initialization functions and configuration structures.

Visual inspection of the configured clock paths is available using the graphical clock tree. The MCUXpresso Clock Tool validates clock settings and provide calculations of the resulting clock frequencies.





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## NXP LPC5500 MCU SERIES MCUXPRESSO CONFIG TOOLS – PERIPHERALS TOOL

#### PERIPHERALS TOOL

The MCUXpresso Peripherals Tool allows users to add desired peripherals to their designs, including UART, ADC, SPI, I<sup>2</sup>C, and more. It will generate initialization structures for the MCUXpresso SDK drivers and offers an easy-to-use quick selection feature which allows starting references to be pre-populated based on peripheral selections. It will also allow the user to easily create example code for USB applications by establishing the configuration of the device and selecting callbacks to implement on top of the existing MCUXpresso SDK middleware and drivers. In addition, users can also quickly validate their selections to confirm that the settings are conflict free, and an alert will call out conflicts when they arise.

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#### MCUXPRESSO SOFTWARE AND TOOLS | CORE TECHNOLOGIES A UNIFIED SUITE OF TOOLS FOR EASY DEVELOPMENT WITH NXP MCUs



MCUXpresso Software and Tools for General Purpose MCUs and Crossover processors



MCUXpresso IDE

Edit, compile, debug and optimize in an intuitive and powerful IDE



## MCUXpresso SDK

Runtime software including peripheral drivers, middleware, RTOS, demos and more



## MCUXpresso Config Tools

Online and desktop tool suite for system configuration and optimization



## MCUXpresso Secure Provisioning Tool

Graphical and command line tool for securely provisioning and programming MCUs with secure boot

MCUXpresso Software and Tools

# ADDITIONAL WEB RESOURCES



# 

MCUXpresso Software and Tools Overview Page: <a href="https://www.nxp.com/mcuxpresso">https://www.nxp.com/mcuxpresso</a>

MCUXpresso Software and Tools Community Site: <a href="https://community.nxp.com/community/mcuxpresso">https://community.nxp.com/community/mcuxpresso</a>



## Support devices

Supported Devices Table (Community Doc)

MCUXPRESSO SOFTWARE AND TOOLS

FreeMASTER page / Community



## SECURE CONNECTIONS FOR A SMARTER WORLD

